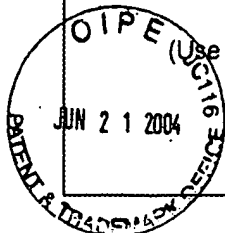


FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S) INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 02EK-108868	SERIAL NO. 10/779,464
	APPLICANT Tzartzanis, et al.	
	FILING DATE: February 13, 2004	GROUP ART UNIT: 2816 2827


REFERENCE DESIGNATION
U.S. PATENT DOCUMENTS

EXAM'R INITIAL		DOCUMENT NUMBER	DATE	NAME	Class	Subclass	Filing Date If Appropriate
	A						
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FOREIGN PATENT DOCUMENTS

EXAM'R INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	Subclass	TRANSLAT'N	
	B						yes	no
	B							

OTHER ART (Include Author, Title, Date, Pertinent Pages, Etc.)

HH	C1	R. Foss, R. Harland, "Peripheral Circuits for One-Transistor Cell MOS RAM's", IEEE Journal of Solid-State Circuits, Vol. SC-10, No. 5, October 1975.
	C2	N. Lu, H. Chao, "Half-V _{dd} Bit-Line Sensing Scheme in CMOS DRAM's" IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 4, August 1984.
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06/21/04

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S) INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 02EK-108868	SERIAL NO. 10/779,464
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WJ	C8	M. Izumikawa, M. Yamashina, "A Current Direction Sense Technique for Multiport SRAM's," IEEE Journal of Solid-State Circuits, Vol. 31, No. 4, April 1996.
	C9	N. Tzartzanis, W. Athas, "Clock-Powered Logic for a 50MHz Low-Power RISC Datapath," IEEE ISSCC Digest of Technical Papers, pp. 338-339, San Francisco, CA, Feb. 6-8, 1997.
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HW	C15	W. Athas, et al., "The Design and Implementation of a Low-Power Clock-Powered Microprocessor," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, Nov. 2000.
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HW	C20	S. Hsu, et al., "A 90nm 6.5GHz 256x64b Dual Supply Register File with Split Decoder Scheme", Symposium on VLSI Circuits, June 2003.

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